A.M.I

Acoustic Mine Imaging

Wet End Controller Card

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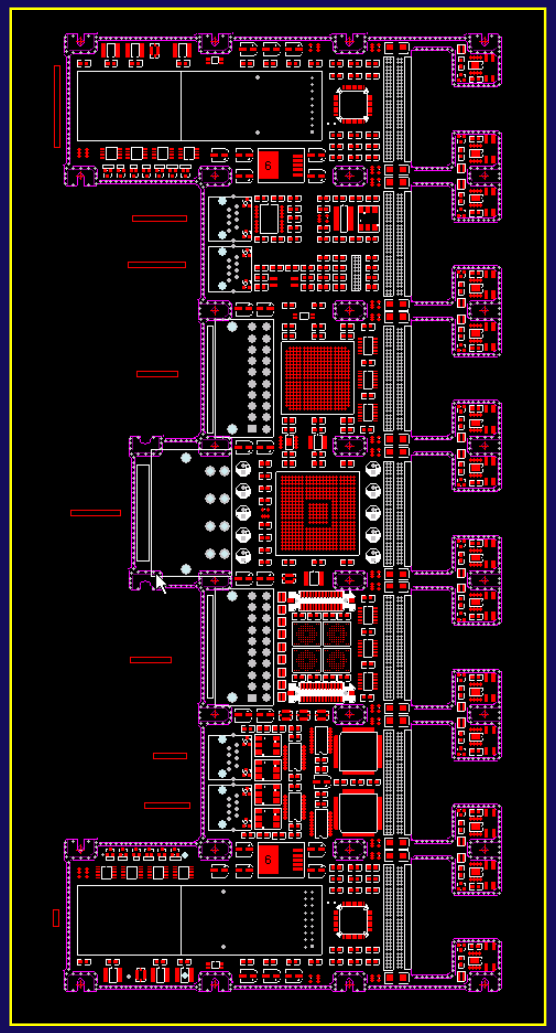
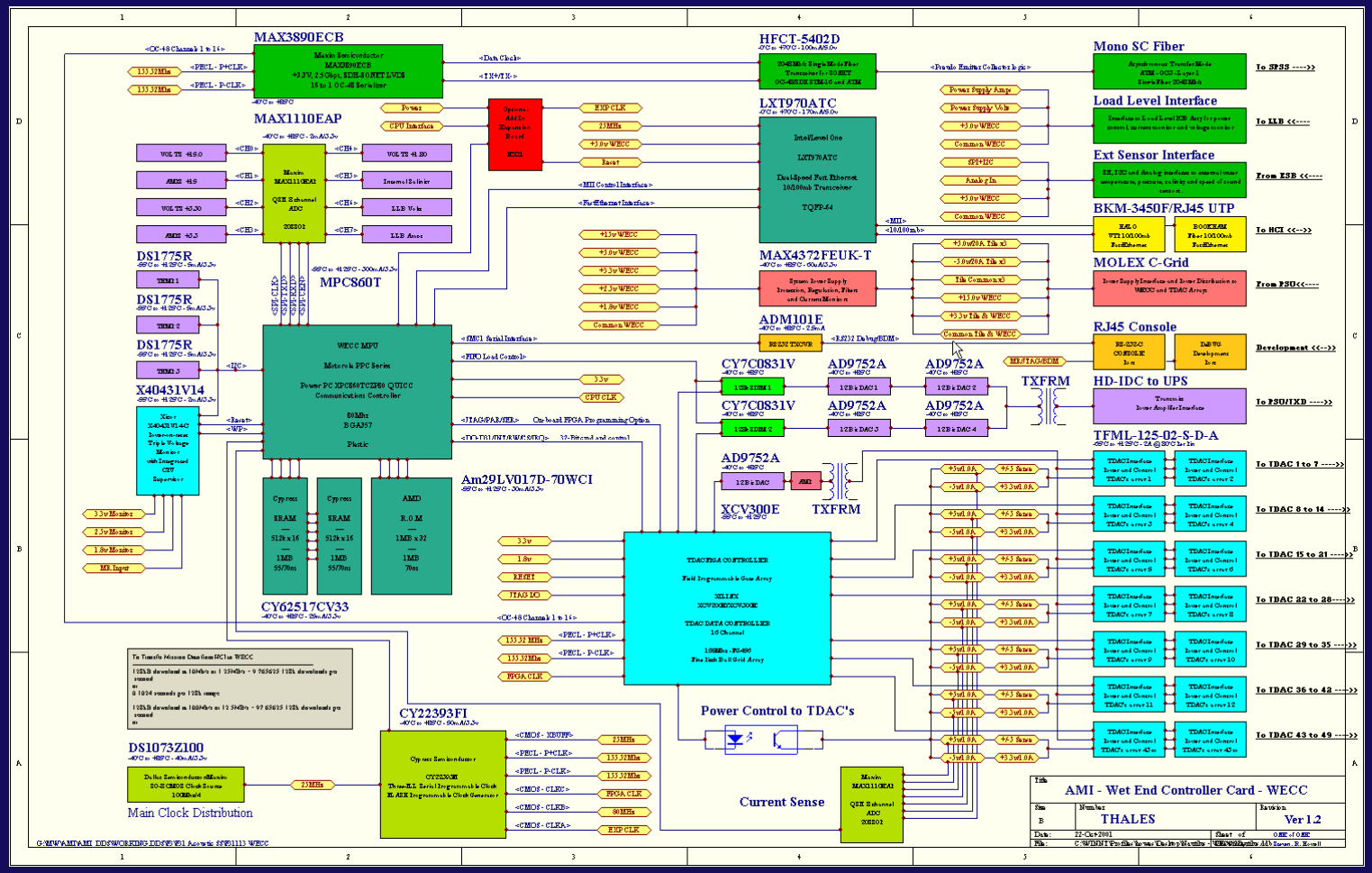
What is the Wet End Controller Card?

The WECC is the principal card located within the *Array Sub-System* at the Wet end of the AMI system.
The task of the WECC, is to control all wet end functions, including the control of sonar acquisitions to the *Signal Processing Sub-System*, and the communication of commands and control to the *Human Computer Interface*. The WECC also makes available vital data regarding the current environmental conditions and the status of the mission.



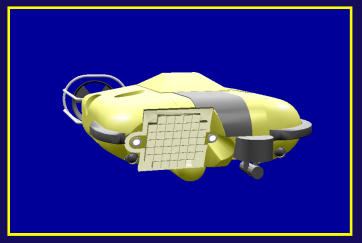
WECC PCB Assembly

WECC - A block Diagram Overview



The overall block diagram of the Wet End Controller Card

The sections that make up the WECC.

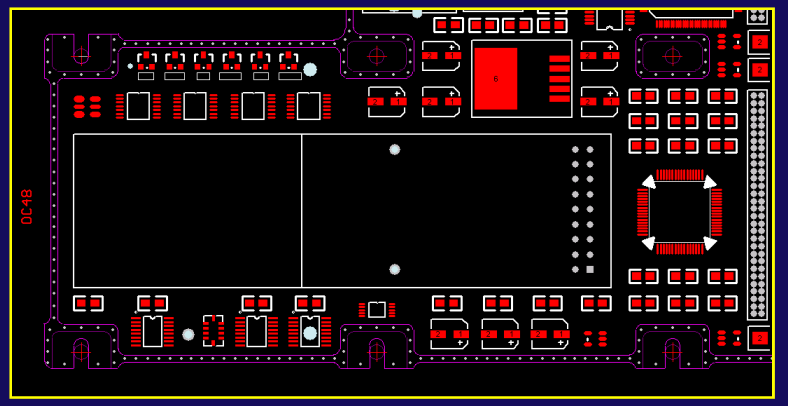


Acoustic Sub System

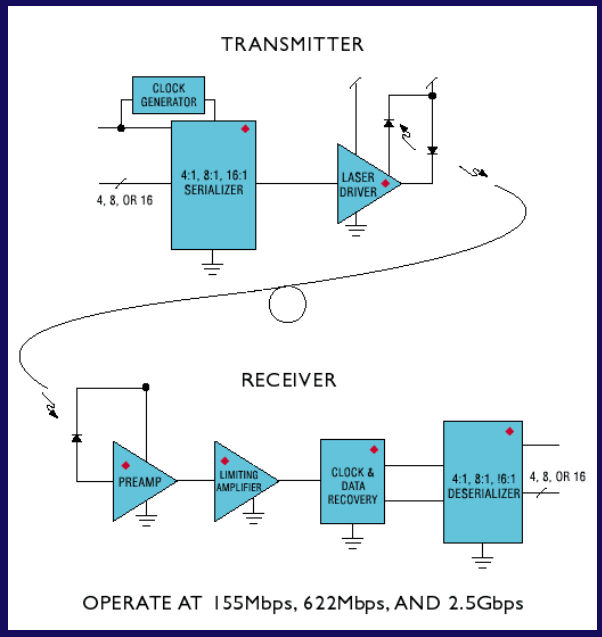
- *Tasks of the WECC*
  - OC-48, 2.44Gbps, 16x 155Mb, ATM Layer 1 Sonar Data Link
  - High speed 10/100Mb Full Duplex, Single Fiber, Ethernet Interface
  - 80MHz PPC Central Processor, for all control functions
  - Programmable FPGA Data Formatter and OC-48 Data Multiplexer
  - Tile Interface and Power Management System
  - Environmental Sensors, Internal and External
  - Sonar Transmitter Signal Generation and DPRAM Setup
  - TVN Noise Envelope Generation system

OC-48 Sonar Data Link

One of the key important features of the WECC, is the OC-48 link. This 2.4Gbps ATM layer 1 compliant interface, configured as 16 channels of 155Mbps, is primarily used for the high-speed data delivery of acquired image information to the SPSS dry end, ready for beam forming.



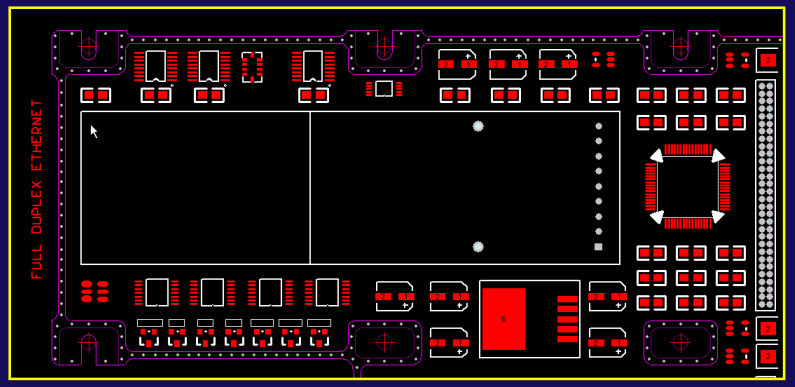
The OC-48 PCB Layout



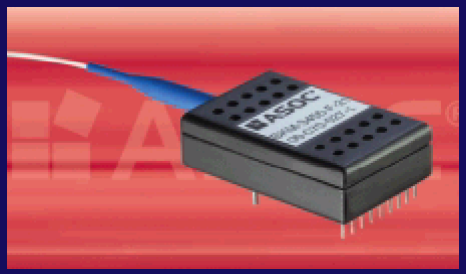
The 2.4Gbps OC-48 Layer 1 Link

High Speed Ethernet

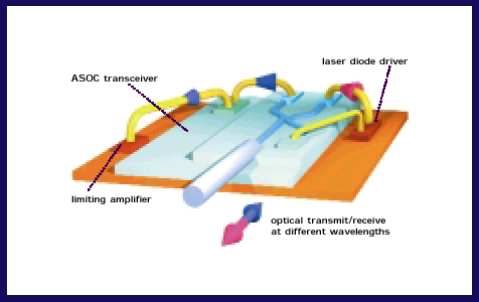
The WECC interface to the HCI is a 10/100Mbps fast Ethernet interface. This high speed, full duplex, TCP/IP based connection, is used for the command and control of the ASS, which is performed over a single mono mode fiber. An additional UTP Ethernet interface is provided for out-of-water services and diagnostics.



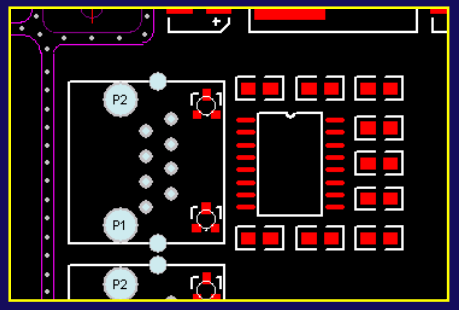
The Single Fiber Ethernet PCB Layout



Single Fiber Transceiver



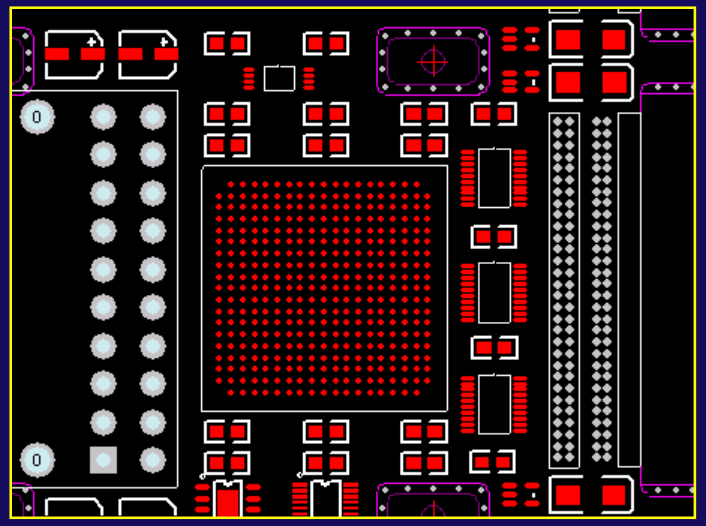
Glass to Silicon ASOC



Additional UTP PCB Layout

PPC Central Processor

The Central processor is an 80MHz PPC embedded QUICC 860T Motorola CPU. The memory capacity is configured as 4MB of SRAM and 16MB of flash, allocated to the LynxOS Firmware. To ensure an electrically quiet operating environment, the CPU is able to enter a deep sleep mode in which all data clocks are stopped. In conjunction with all memory devices being SRAM technology, this minimizes cross-talk of electrical noise into the acquired sonar data.

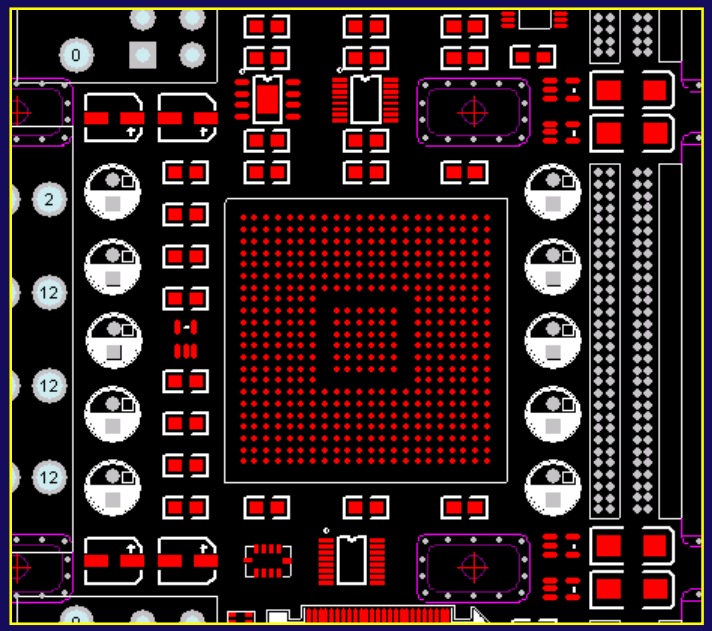


CPU PCB Layout

The MPC860 CPU

Programmable FPGA

A key peripheral to the WECC is the high speed "state machine" FPGA, which is responsible for the formatting and delivering of the image data to the dry end, via the OC-48 data link. This high-speed device allows extremely efficient operation and offers quiet electrical characteristics. Whilst sampling data, all clocks are “locked” to the sample rate, which reduces the likelihood of alias, other than DC.

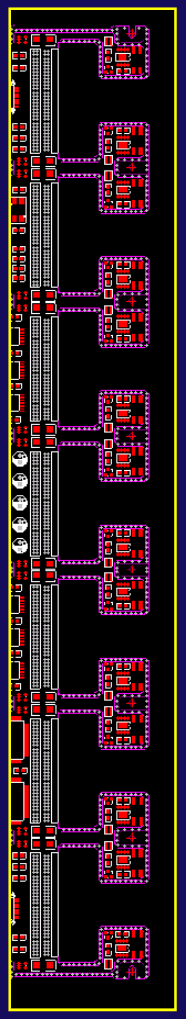


FPGA PCB Layout

The Xilinx FPGA

VIRTEX

Virtex FPGA Technology



Tile Interface PCB Layout

Tile Interface and Power Management

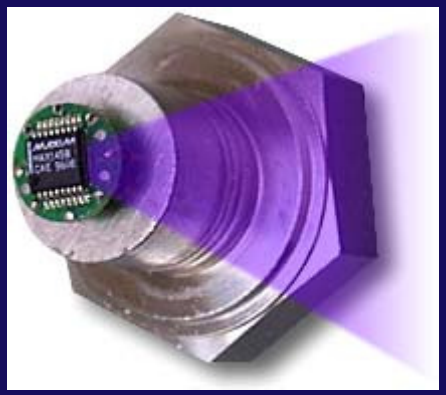
The WECC provides an interface to each of the 45 acquiring hydrophone TDAM's. These interfaces provide both mechanical and electrical services that make the interconnection of a large array a simple and reliable task. The WECC also manages the collapsed power distribution and control amongst the tile arrays.

Tile Interface and associated TDAM Layout

Environmental Sensors

The WECC has a series of internal and external sensors available to monitor the local environment. Sensors for temperature, salinity and water pressure allow the determination of "speed of sound", providing important information for a quality image acquisition. In addition, integral sensors to the power supplies and other circuits, ensures correct electrical operation.

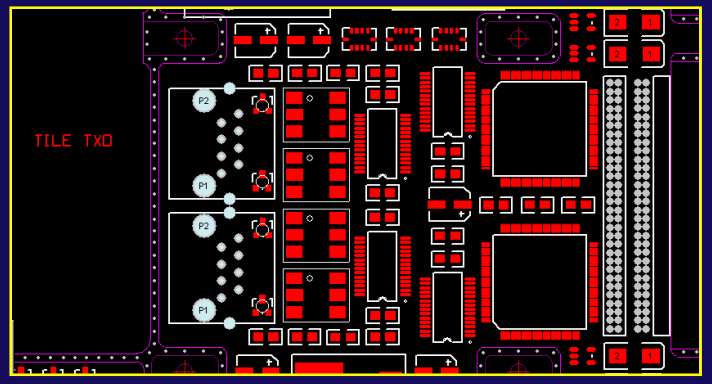
Temperature Sensors



External Pressure Sensor

Sonar Transmitter and DPRAM's

The sonar transmitter circuit creates the analogue waveforms that "ping" off the object being imaged. By utilizing a 128k deep DPRAM, four different sonar transmission functions are supported. Theses are Manoeuver, for Near (190kHz), Medium (190kHz) and Far (110kHz), plus a Zoom function (850kHz). Whilst acquiring data, the processor is placed into a deep sleep mode, creating an ideal quiet operating environment.



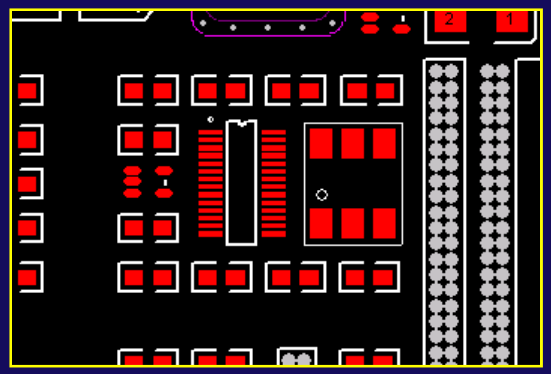
TxDAC and DPRAM PCB Layout

TxDAC Transmitter DAC

High Speed "Dual Ported Random Access Memories"

TVN Noise Generator

The TVN circuits are responsible for creating and distributing the time varying noise envelope used in the data acquisition by the *Tile Data Acquisition Modules*. As part of the sonar data, precisely generated time varying noise is injected into the data samples. This dithers the sonar data giving a more accurate digitization of the signal when quantized to one bit values by the TDAM.

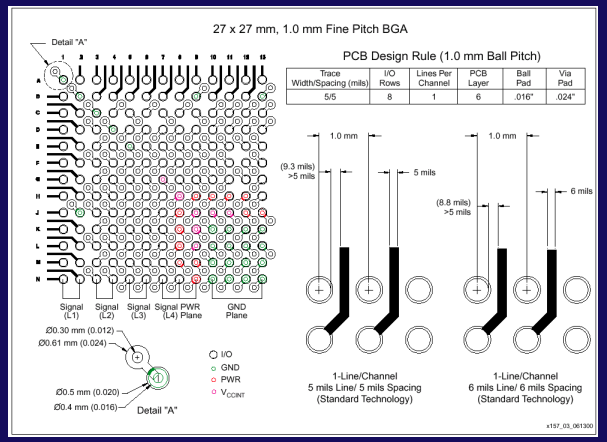


TVN PCB Layout

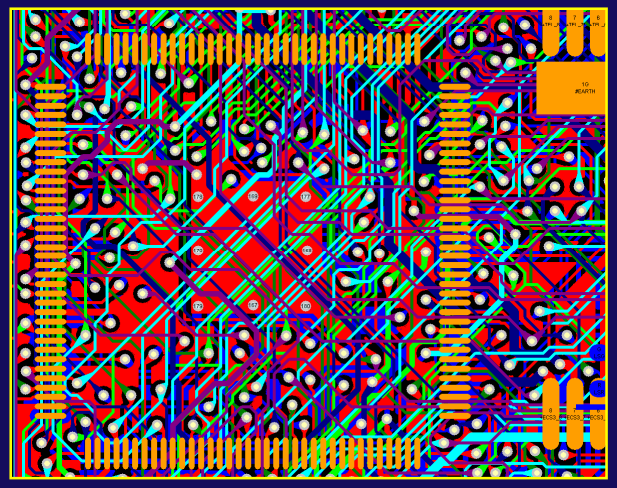
Digital-to-Analog

Manufacture and Assembly

The WECC utilizes leading edge design and manufacturing technologies to simplify and make possible, the production of this system. By ensuring the product is compliant with modern manufacturing and testing techniques, the WECC can be manufactured with little, to no complications.



Ball Grid Array Routing Plans



PCB 5/5 Routing Technology

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Thank You

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